Cryptography Conference

Accelerated Quantum Supercomputing and Post-Quantum Cryptography

Accelerated computing is revolutionizing numerous fields, including quantum computing (QC) and artificial intelligence (AI), and is also set to accelerate the development of robust post-quantum cryptographic solutions. This talk explores how cutting-edge AI techniques are addressing challenges within QC across the hardware and software stack to create more optimized circuits, bringing practical quantum computers one step closer. Additionally, this talk will cover how GPU-based acceleration serves as a safeguard against emerging quantum cryptographic threats. We will reveal how GPU-based algorithms are accelerating cryptographic research by examining technical challenges in parallelizing cryptographic workloads across GPUs, managing memory bandwidth, optimizing performance, and overcoming hardware limitations. We will also highlight how these technologies are accelerating QC research. Real-world applications in sectors such as finance, healthcare, and data privacy will be showcased, demonstrating the practical benefits of AI, QC, and PQC.



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Accelerated Quantum Supercomputing and Post-Quantum Cryptography

Yarkin Doroz – Product Manager

Post-Quantum Cryptography Conference PKI Consortium

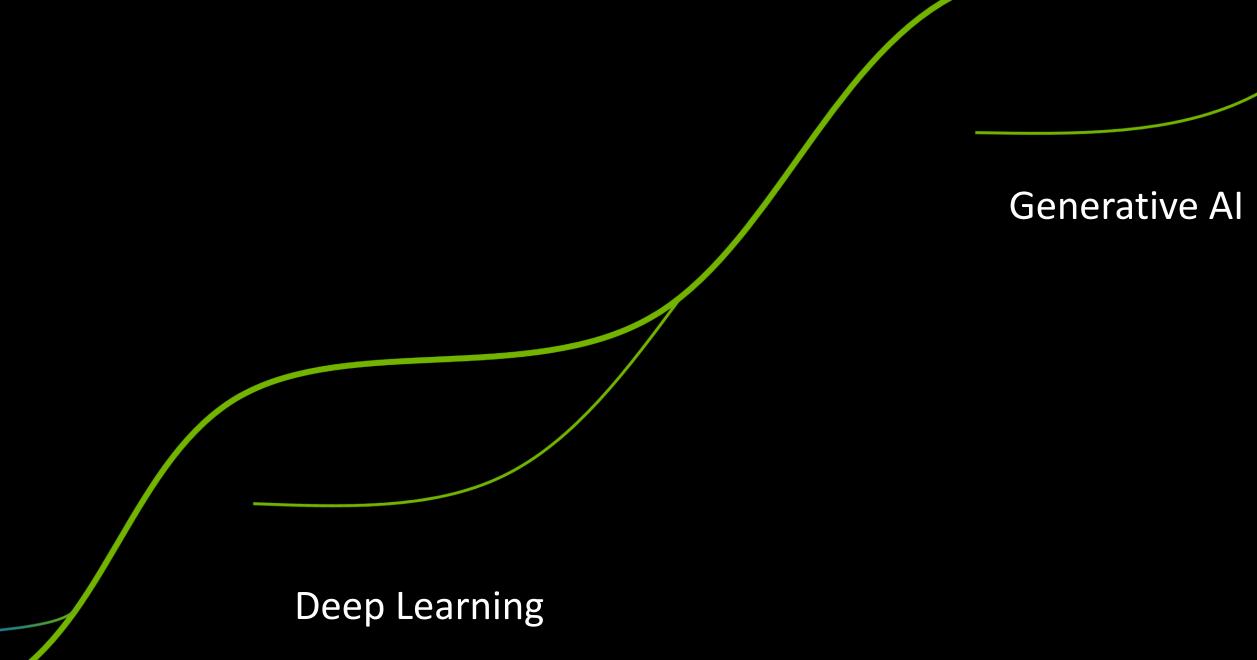


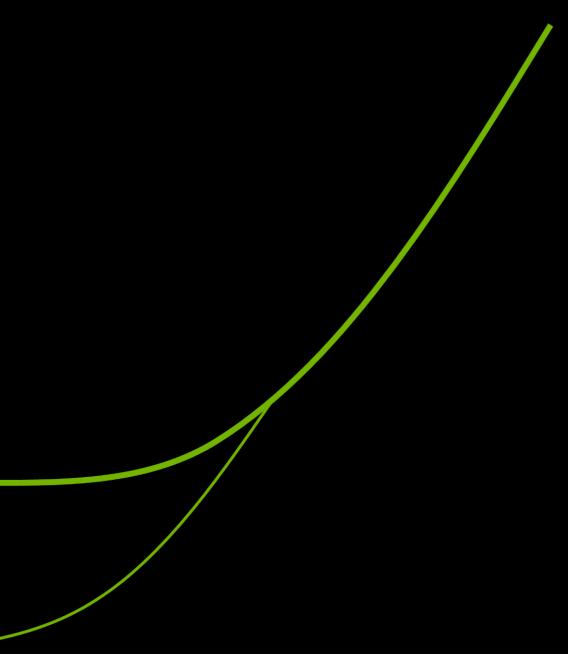




Scientific Computing

Computing Revolutions







Scientific Computing

Computing Revolutions

Generative Al

Deep Learning

Quantum Computing





NVIDIA is not building Qubits





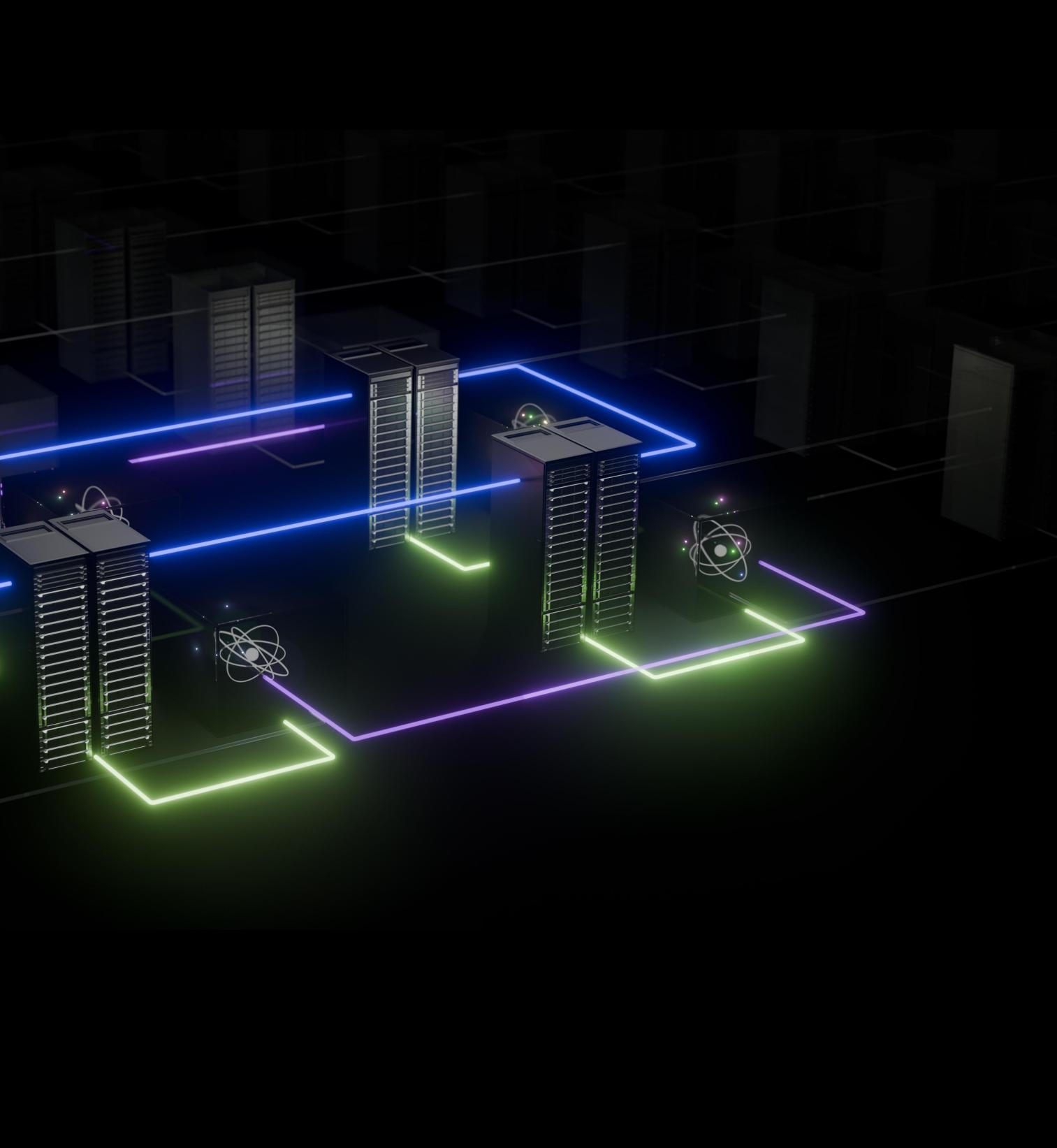
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NVIDIA is building all **Accelerated Quantum Supercomputers**

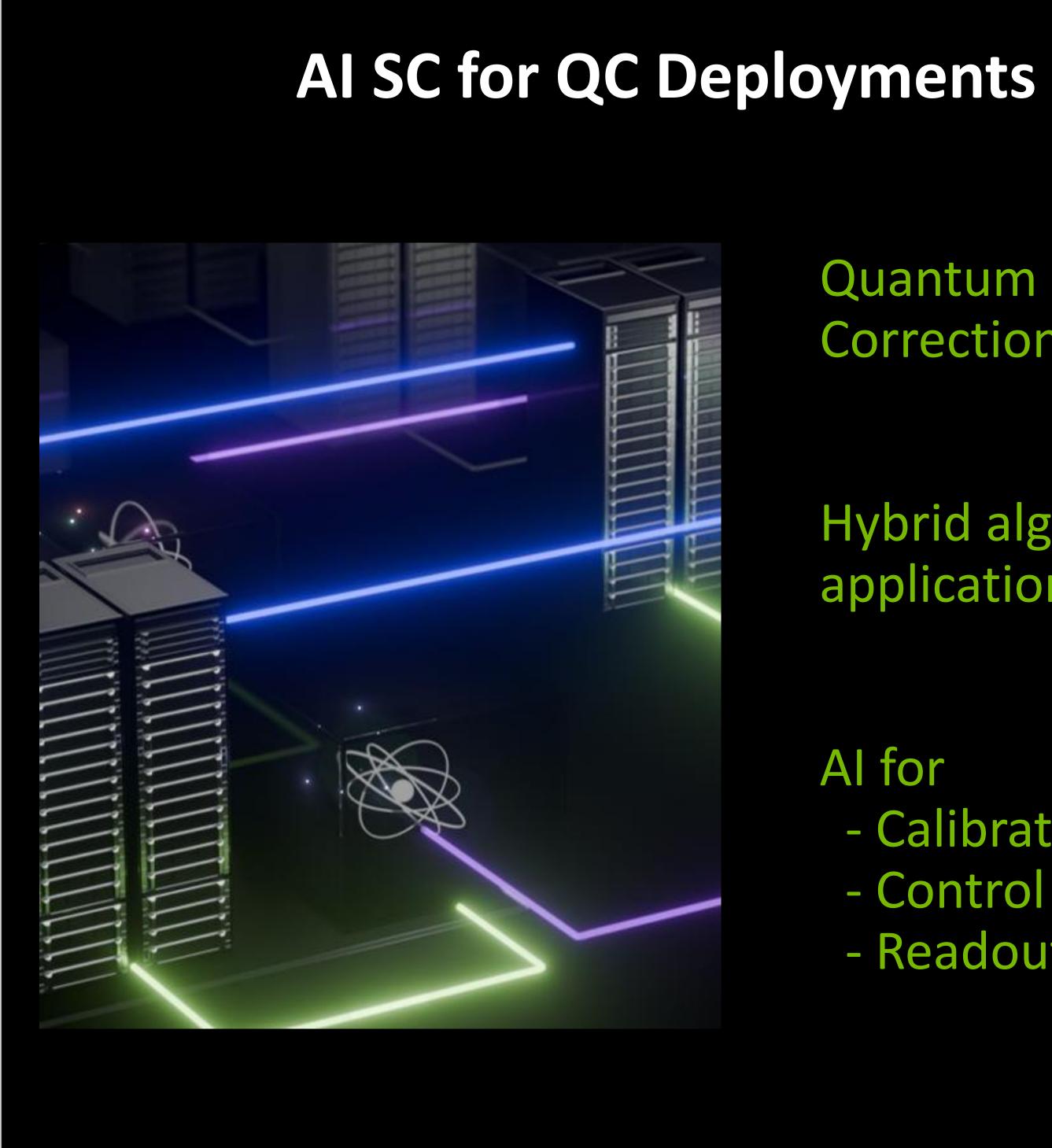
The Accelerated Quantum Supercomputer

- Supercomputing architecture connecting quantum hardware
- Ability to run hybrid algorithms using GPUs and QPUs
- A software platform that seamlessly connects hybrid applications
- The ability to perform qubit-agnostic development of control and error correction





Quantum Computing Needs Accelerated Computing



- Quantum Error Correction
- Hybrid algorithms and applications
- Al for
- Calibration
- Control
- Readout



AI SC for QC Development

Accelerated application development

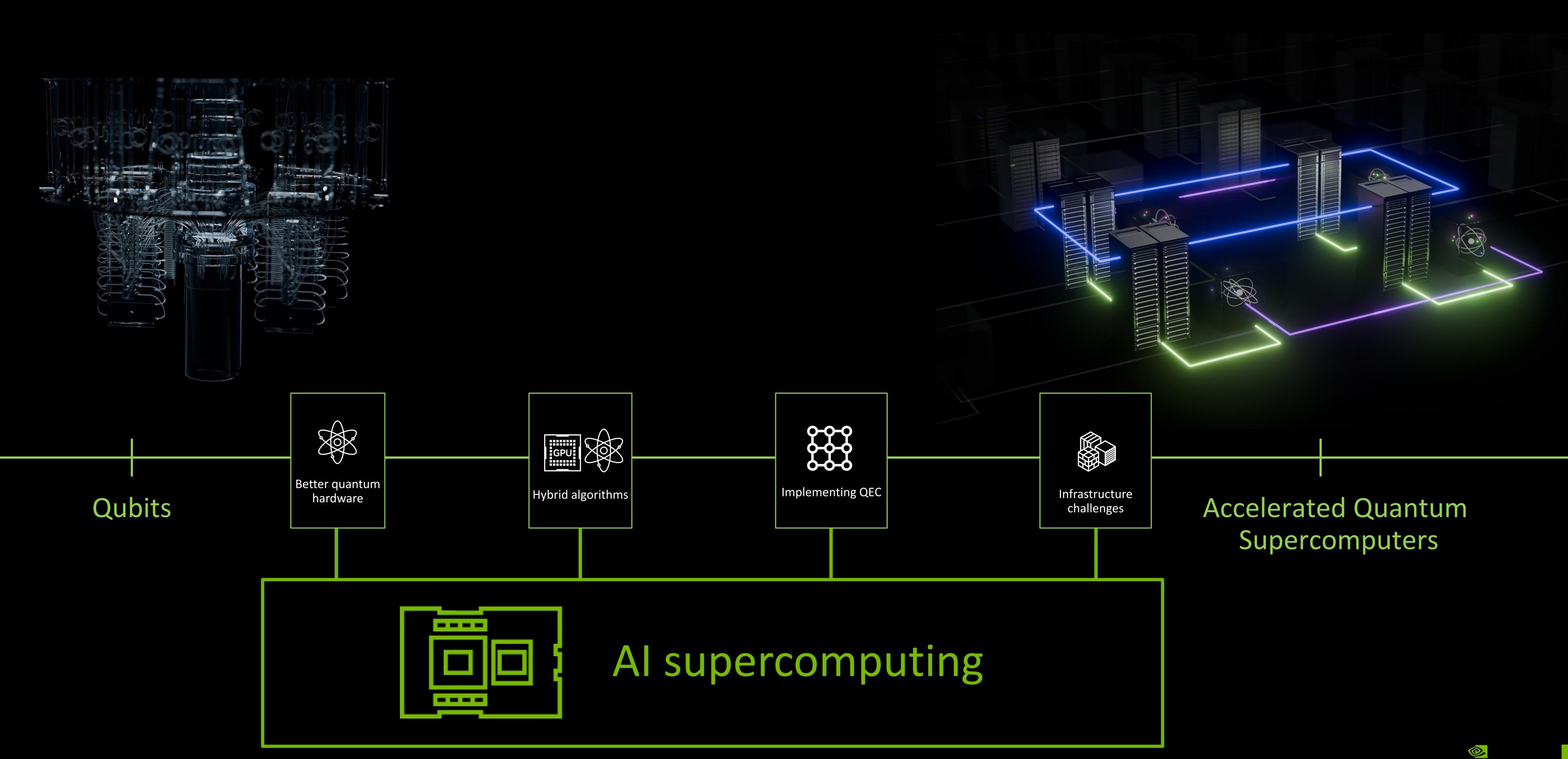
Al assisted circuit design

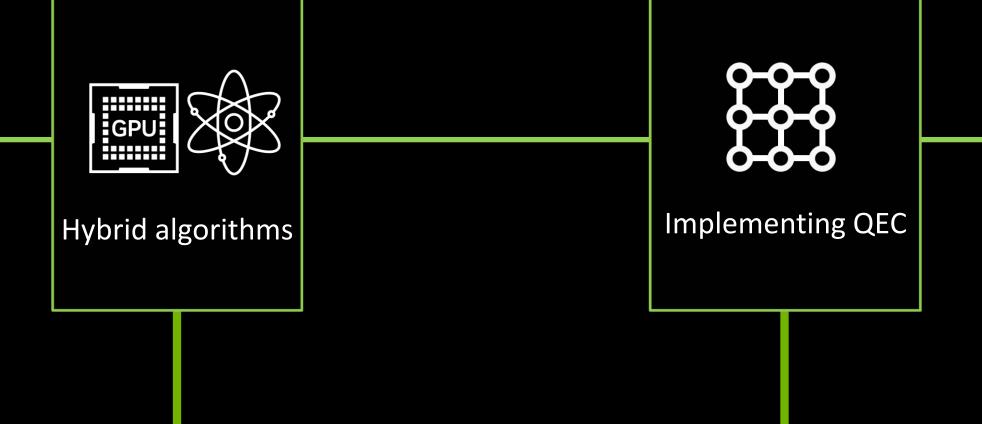
Dynamical simulations

Noise modeling



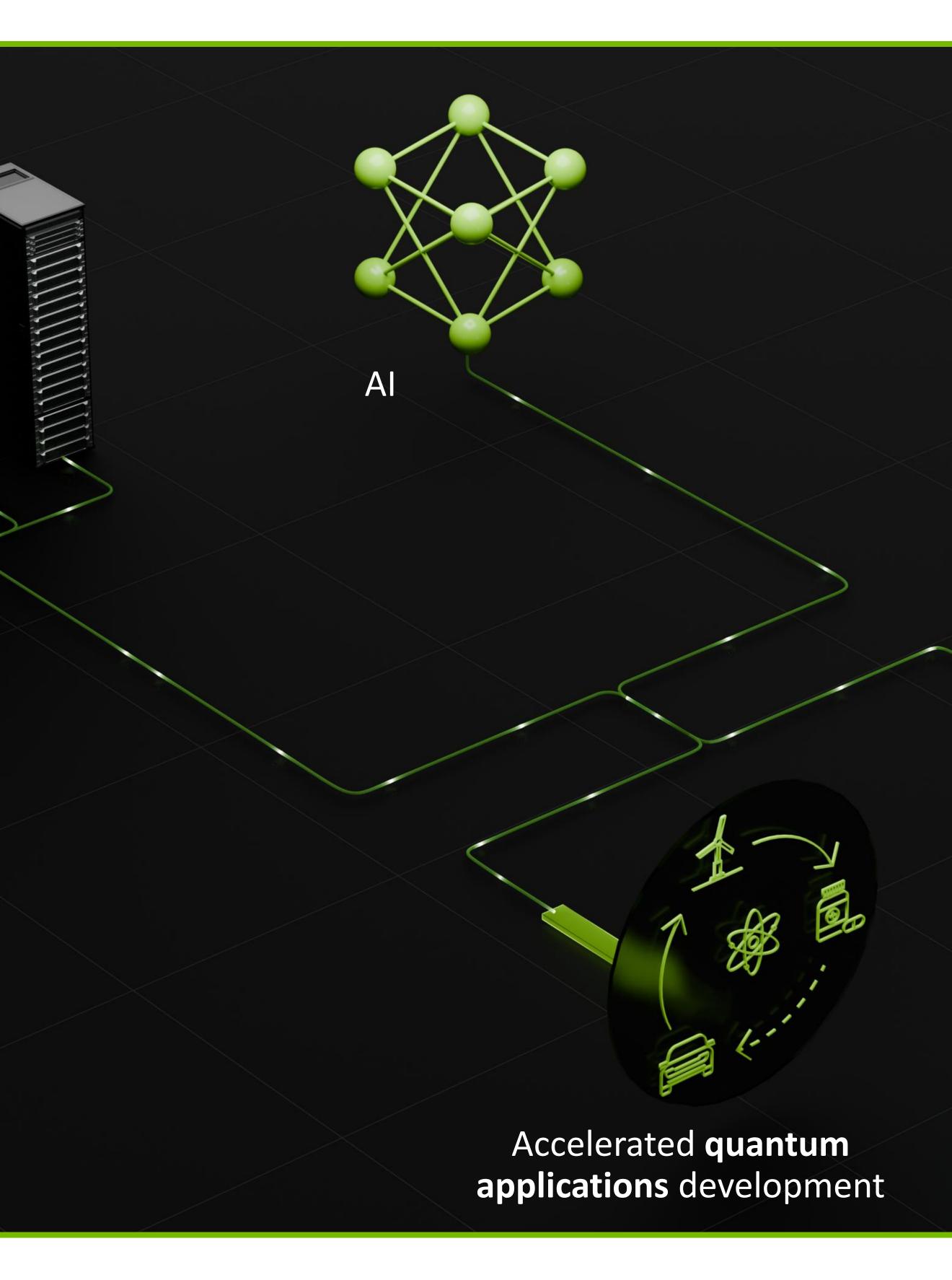
Accelerating the Journey From Qubits to Supercomputers





Al Supercomputing

Bringing AI to quantum computing





Accelerated quantum hardware development



Artificial Intelligence for Quantum Computing

Benjamin^{5,6}, Zhenyu Cai^{5,6}, Zohim Chandani¹, Federico Fedele², Nicholas Harrigan¹, Jin-Sung Kim¹, Elica Kyoseva¹, Justin G. Lietz¹, Tom Lubowe¹, Alexander McCaskey¹, Roger G. Melko^{7,8}, Kouhei Nakaji¹, Alberto Peruzzo⁹, Sam Stanwyck¹, Norm M. Tubman¹⁰, Hanrui Wang¹¹ and Timothy Costa¹ 95051, CA, USA. Road, Oxford, OX1 3PJ, United Kingdom. and Engineering, and Chemical Engineering and Applied Science, University of Toronto, 80 St George St, Toronto, M5S 3H6, ON, Canada. ⁴Vector Institute for Artificial Intelligence, 661 University Ave Suite 710, Toronto, M5G 1M1, ON, Canada. ⁵Quantum Motion * 9 Sterling Way, London, N7 9HJ, United Kingdom. ⁶Department of Materials, University of Oxford, Parks Road, Oxford, OX1 3PH, United Kingdom. 200 University Avenue West., Waterloo, N2L 3G1, ON, Canada. North, Waterloo, N2L 2Y5, ON, Canada. ⁹Qubit Pharmaceuticals, 29, rue du Faubourg Saint Jacques, Paris, 75014, France. ¹⁰NASA Ames Research Center, Moffett Field, California,

Yuri Alexeev^{†1}, Marwa H. Farag^{†1}, Taylor L. Patti^{†1}, Mark E. Wolf^{†1*}, Natalia Ares², Alán Aspuru-Guzik^{3,4}, Simon C. ¹NVIDIA Corporation, 2788 San Tomas Expressway, Santa Clara, ²Department of Engineering Science, University of Oxford, Parks ³Department of Chemistry, Computer Science, Materials Science ⁷Department of Physics and Astronomy, University of Waterloo, ⁸Perimeter Institute for Theoretical Physics, 31 Caroline Street

94035-1000, USA.



- Platform design
- Gate and Pulse optimization

Section 2: QC Hardware Development and Design

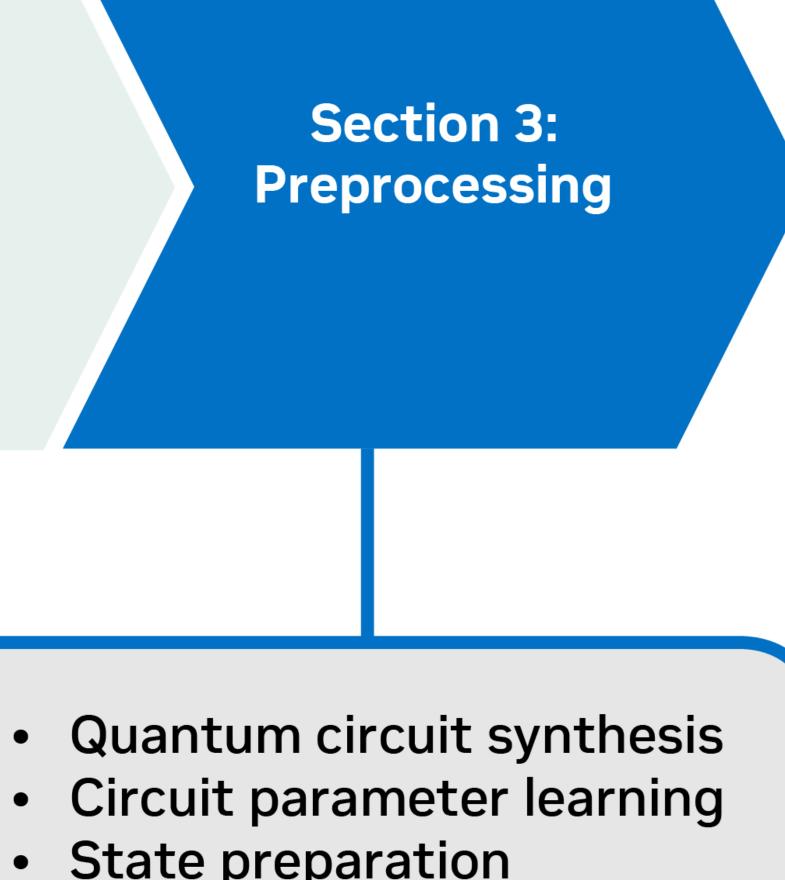
Al for QC



- Platform design
- Gate and Pulse optimization

- State preparation

Al for QC



-



- Platform design
- Gate and Pulse optimization

 Quantum circuit synthesis Circuit parameter learning State preparation

•••

Al for QC



- Qubit control
- Device characterization

Section 4: **Device Control** and Optimization



- Platform design
- Gate and Pulse optimization

 Quantum circuit synthesis Circuit parameter learning State preparation

1 A A A

Al for QC

- Device tuning
- Qubit control
- Device characterization

 QEC decoding Code discovery

Section 5: **Quantum Error** Correction



- Platform design
- Gate and Pulse optimization

 Quantum circuit synthesis Circuit parameter learning State preparation 1.1.1.1

Al for QC

- Device tuning
- Qubit control
- Device characterization

QEC decoding

- Observable estimation and tomography
- Qubit Readout
- Error mitigation

Section 6: Postprocessing

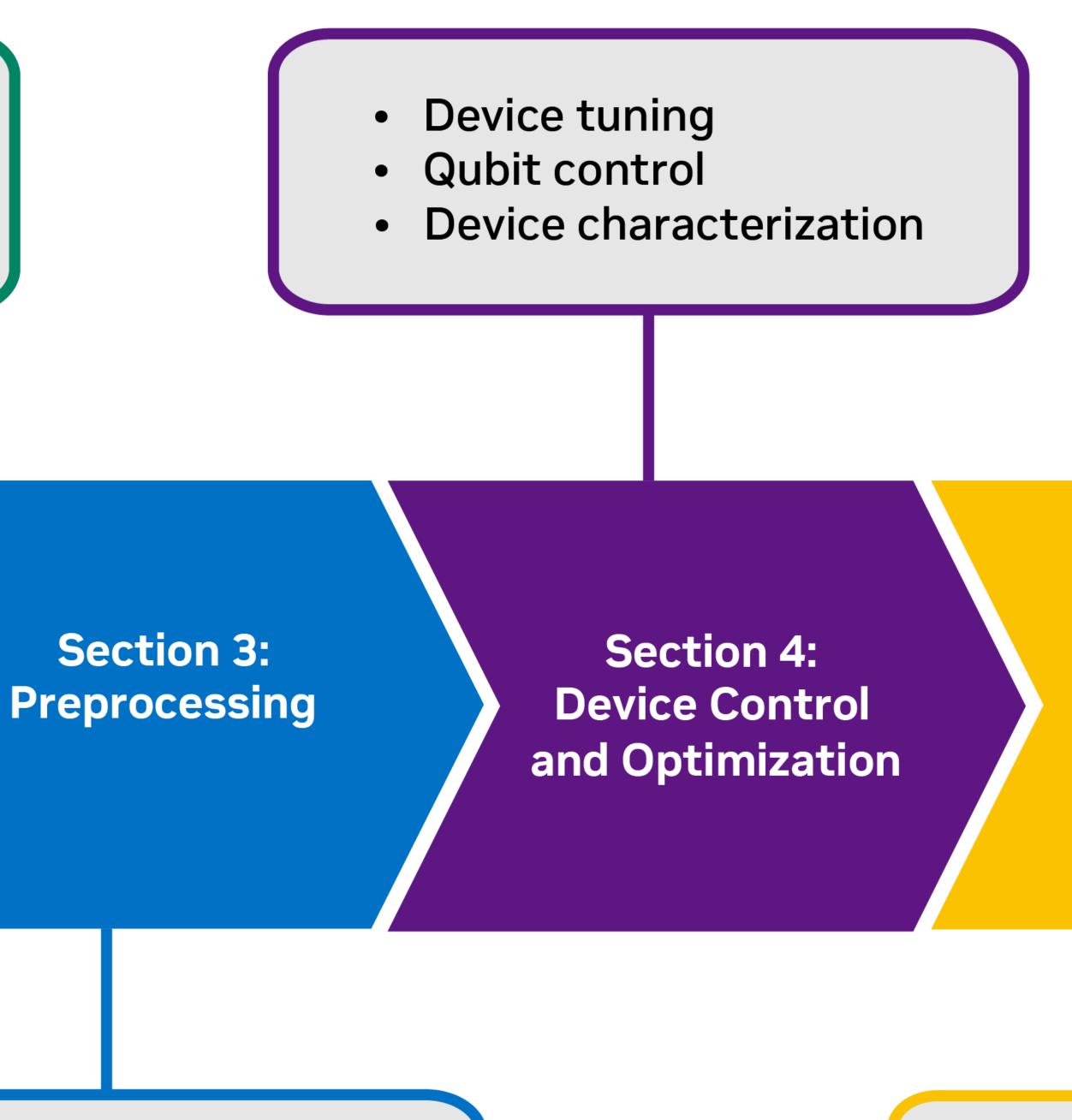


- Platform design
- Gate and Pulse optimization

Section 2: QC Hardware Development and Design

- State preparation

Al for QC



• Quantum circuit synthesis Circuit parameter learning • QEC decoding Code discovery

- Observable estimation and tomography
- Qubit Readout
- Error mitigation

Section 5: **Quantum Error** Correction

Section 6: Postprocessing





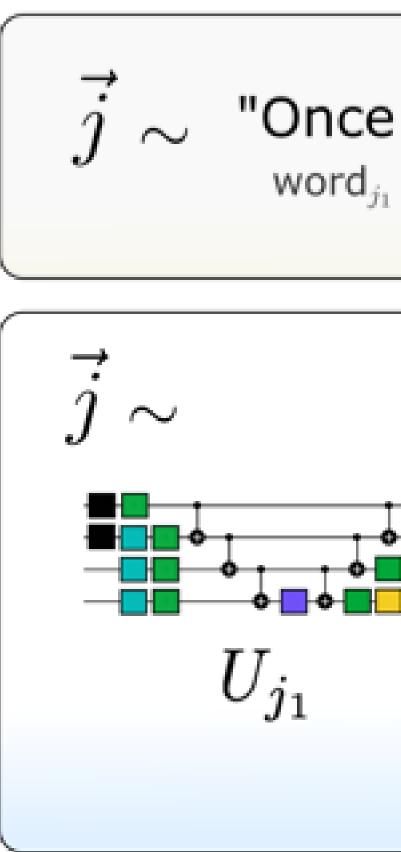
Challenge

- Variational quantum algorithms offered promise for running drug-discovery applications on small quantum devices - but suffer from serious optimization issues
- Many of these problems are tied to how circuits are parametrized.

Solution

- The generative quantum eigensolver acts like a Large Language Model – but generating quantum circuits from quantum operations, rather than sentences from words.
- Using a generative model like GPT to create quantum circuits avoids the limitations of traditional variational quantum algorithms

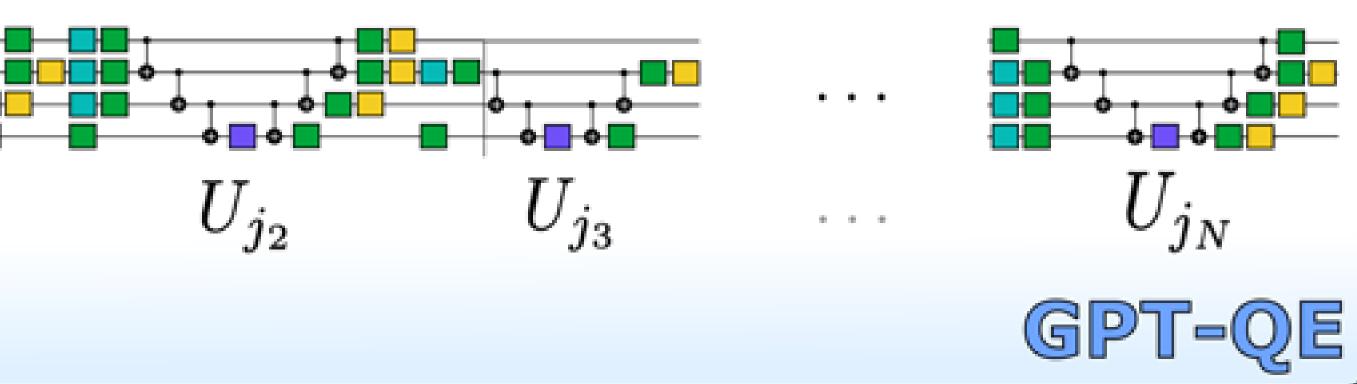
The Generative Quantum Eigensolver First demonstration of GPT-generated circuits





New approach in Using AI for building quantum applications

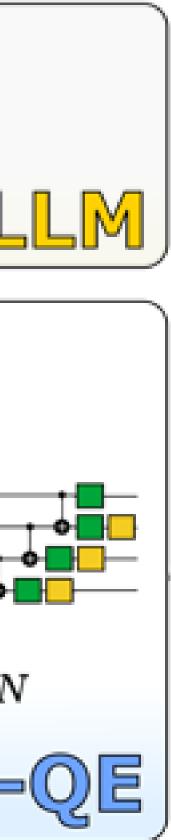
"Once upon a time $\cdot \cdot \cdot$ happily ever after" word_{j_1} word_{j_2} word_{j_3} word_{j_4} \cdots word_{j_{N-2}} word_{j_{N-1}} word_{j_N}





Can be extended to various application areas

Speedup over CPU when running GQE on GPU









Quantum Computers and Quantum Algorithms

- Quantum Computers compute using qubits
- Quantum gates operate on qubits to run Quantum Algorithms
- computations

Two main Quantum Algorithms Related to Cryptography:

Grover's Algorithm

- Quantum Search Algorithm
- Search for an input in an unstructured database
- Reduces complexity from $O(N) \rightarrow O(\sqrt{N})$

Shor's Algorithm

- Quantum Algorithm for Integer Factorization
- Factorize a given integer into its prime factors
- Reduces complexity from $O(N) \rightarrow O(\log_2 N)$

• Phenomena like superposition and entanglement allow qubits to accelerate some





Round 2 **KEMS: 17 DSA: 9** (Jan 2019)

NIST PK-PQC Call (Dec 2016)

Round 1 Submissions **KEM: 59** DSA: 23 (Nov 2017)

NIST PQC Standardization Timeline

Urgency for New Cryptographic Solutions

Finalists **KEM: 1 DSA: 3** (July 2022)

Round 3 Main Candidates **KEM: 4 DSA: 3** Alternatives **KEM: 5 DSA: 3** (July 2020)

Additional DSA - Round 1 DSA: 40 (June 2023)

Round 4 **KEM: 4** (July 2022) Additional DSA - Round 2 DSA: 14 (Oct 2024)



Algorithms

ECDSA, EdDSA, RSA

ECDSA, EdDSA, RSA

Finite Field/Elliptic Curve DH and MVQ, RSA Finite Field/Elliptic Curve DH and MVQ, RSA

NIST PQC Transition Timeline

| Parameters | Depreciate | Disallowed |
|------------|------------|------------|
| 112 | 2030 | 2035 |
| 128 | | 2035 |
| 112 | 2030 | 2035 |
| 128 | | 2035 |



Critical Applications Demanding High-Throughput Post-Quantum Cryptography

Key S

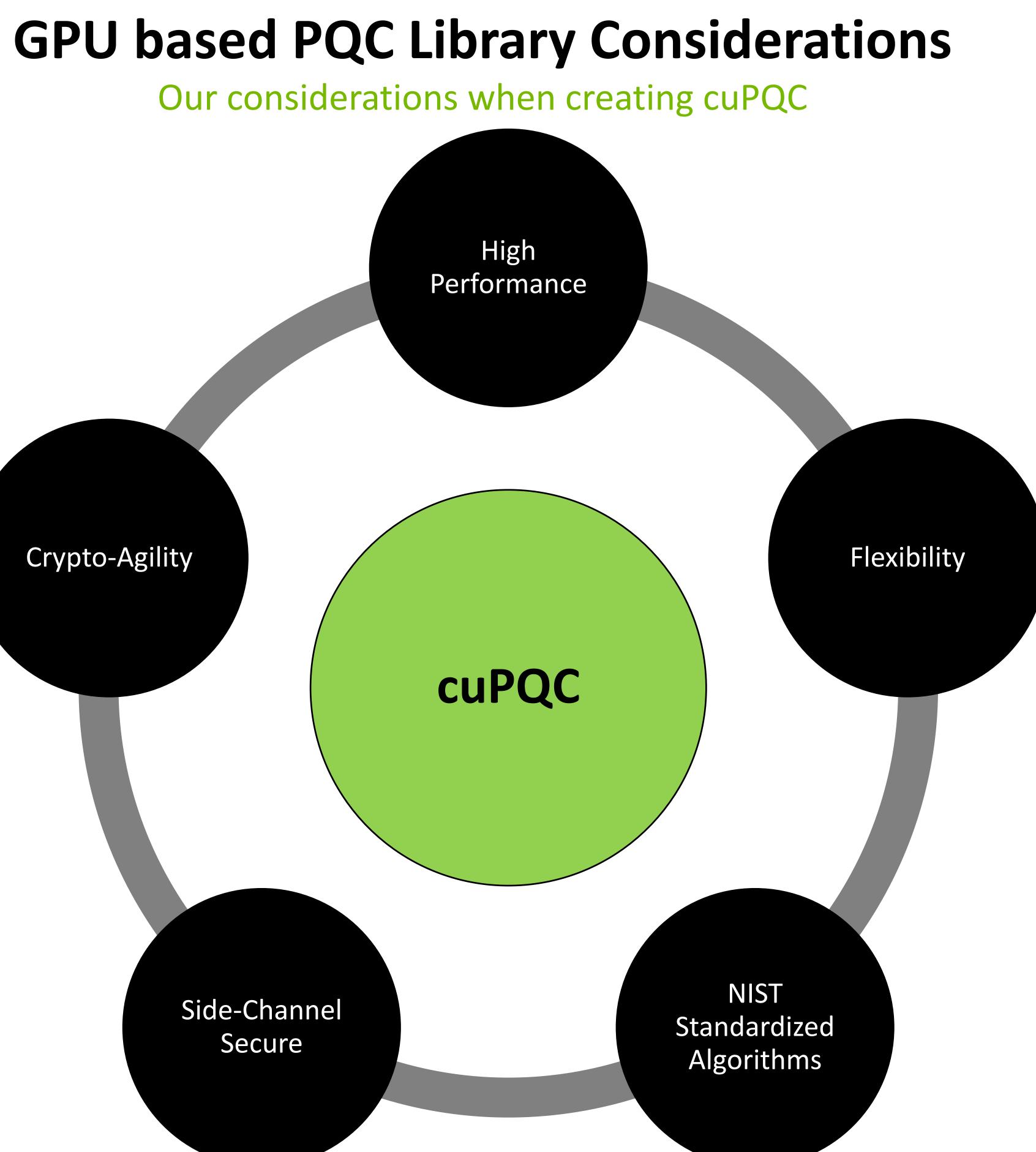
Cloud Service Providers Content Delivery Networks (CDNs) Financial Institutions Telecommunications Companies Military and Government Applicat Blockchain Companies Healthcare Systems **Big Data Analytics Companies** Autonomous Systems **Network Equipment Providers** Internet of Things (IoT) Companies

| Sectors | |
|---------|----------------------------|
| | |
| s) | |
| | TLS (Transport Layer Secu |
| | IPsec (Internet Protocol S |
| ations | SSL (Secure Sockets Laye |
| | SSH (Secure Shell) |
| | HTTPS (Hypertext Transfe |
| | GSM/3G/4G/5G Encrypt |
| | SNMPv3 (Simple Networ |
| | |
| es | |
| | |

Protocols

- curity)
- Security)
- er)
- fer Protocol Secure)
- tion Protocols
- ork Management Protocol version 3)

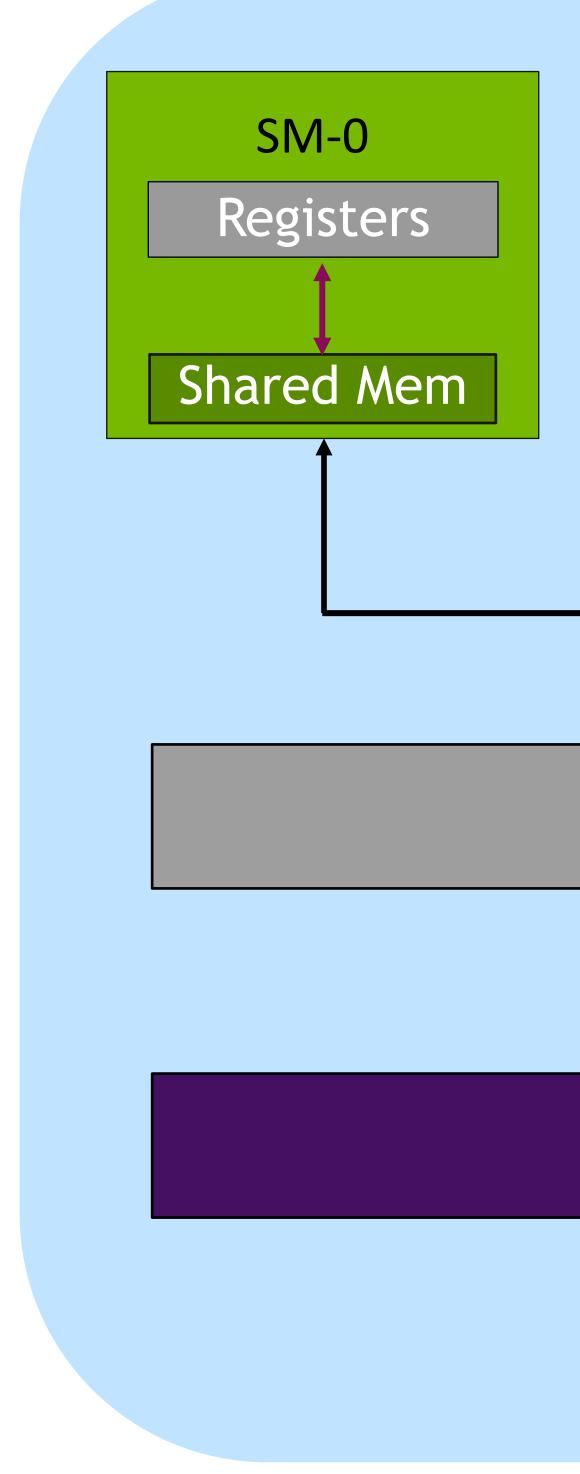


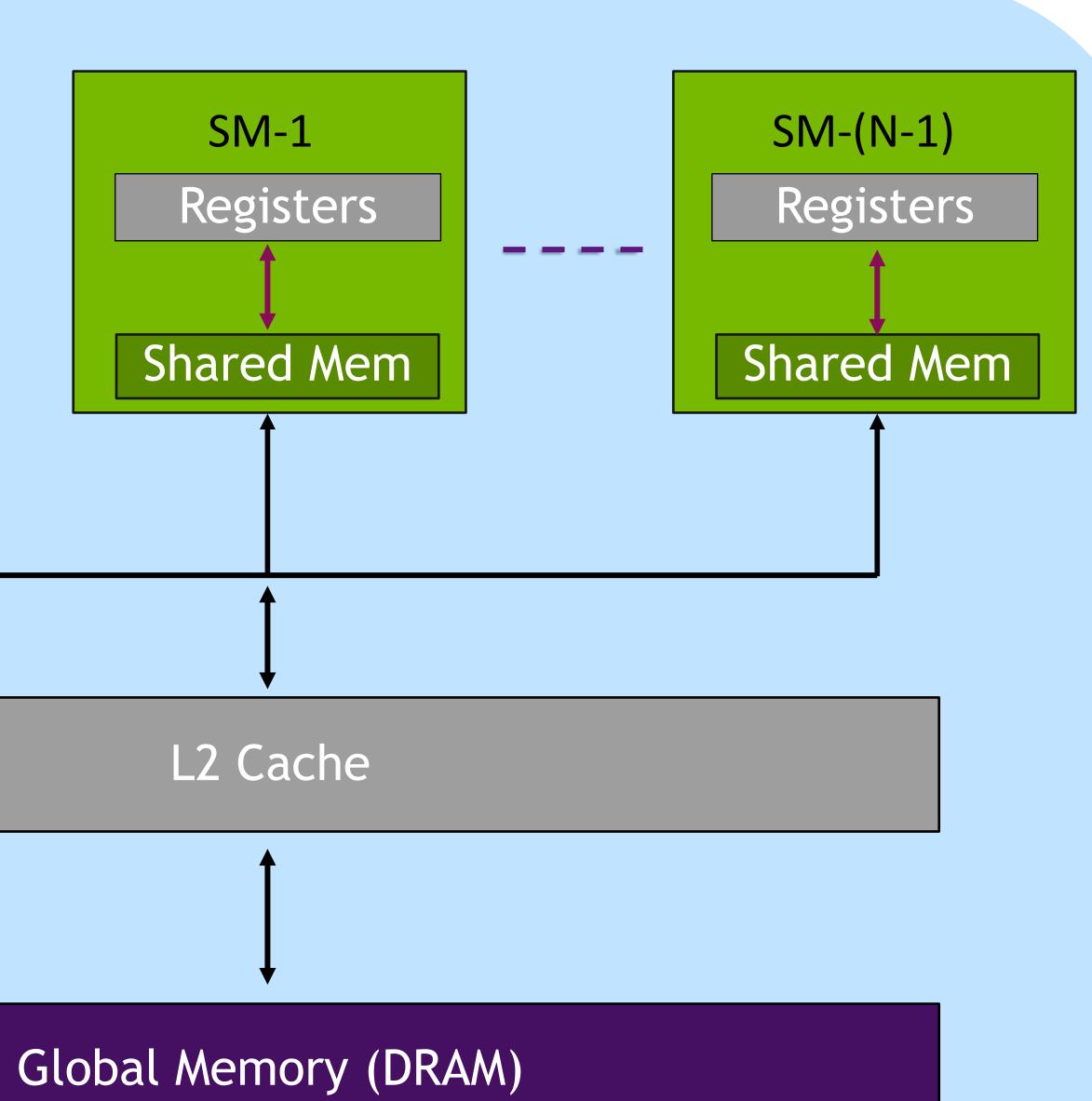




- Certain mathematical subroutines are suitable for parallelization
 - Number Theoretic Transform
- Shared Memory used for collaboration of cores and accelerate mathematical subroutines
 - This space allows threads to work together to solve a larger problem.
- Optimization techniques to allow register-heavy components to be spread across multiple threads.
- Limiting data transfers between the CPU and GPU
 - CPU main memory transfers over PCIE take up valuable clock cycles.
- ML-KEM and ML-DSA are register-use heavy and can limit utilization.
 - Hashing algorithms utilizing Keccak, random sampling, and others.
 - Algorithms need to be reorganized with hardware considerations.

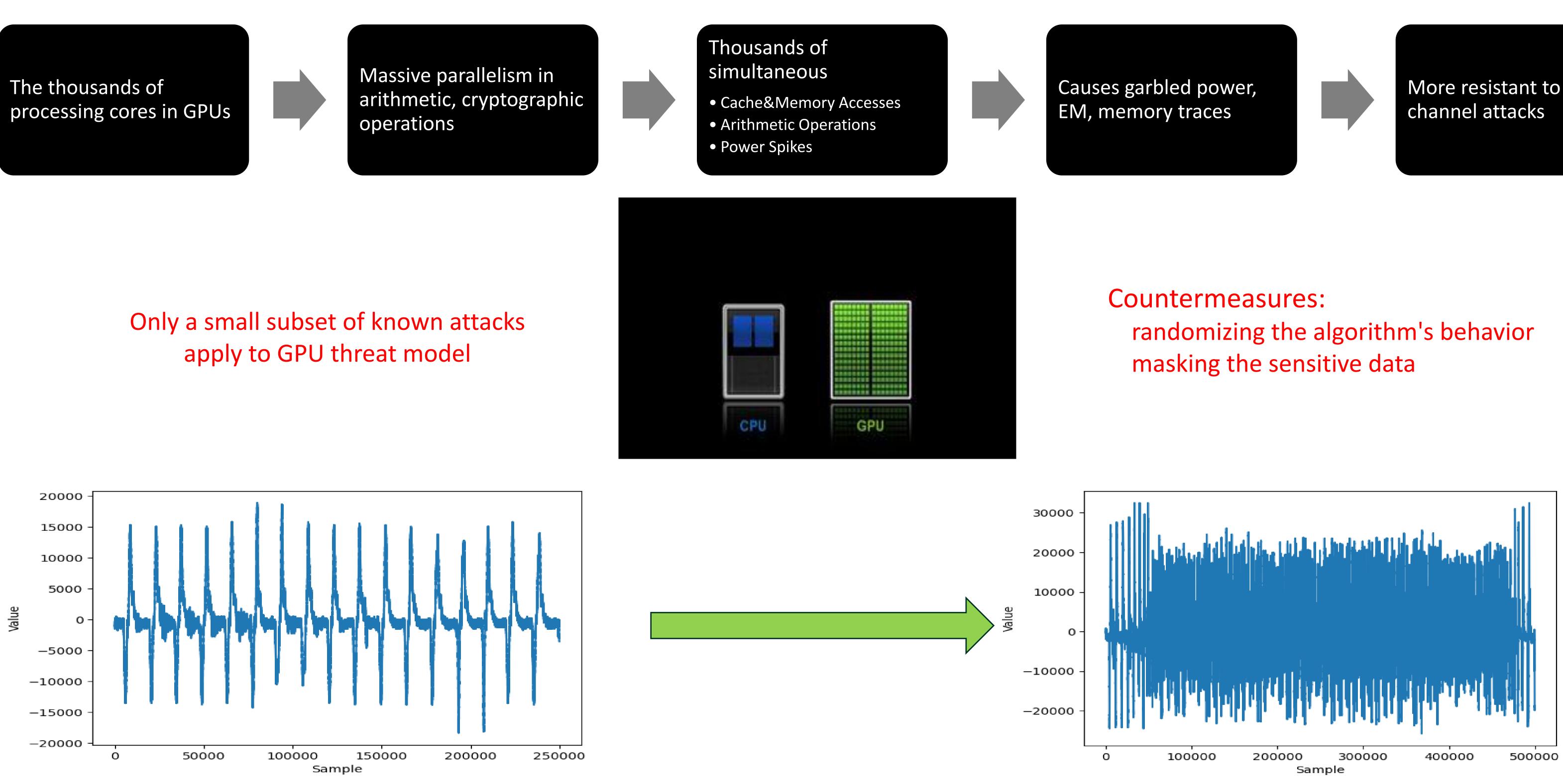
GPU Hardware Optimizations

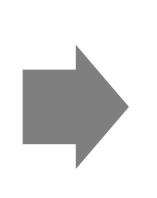






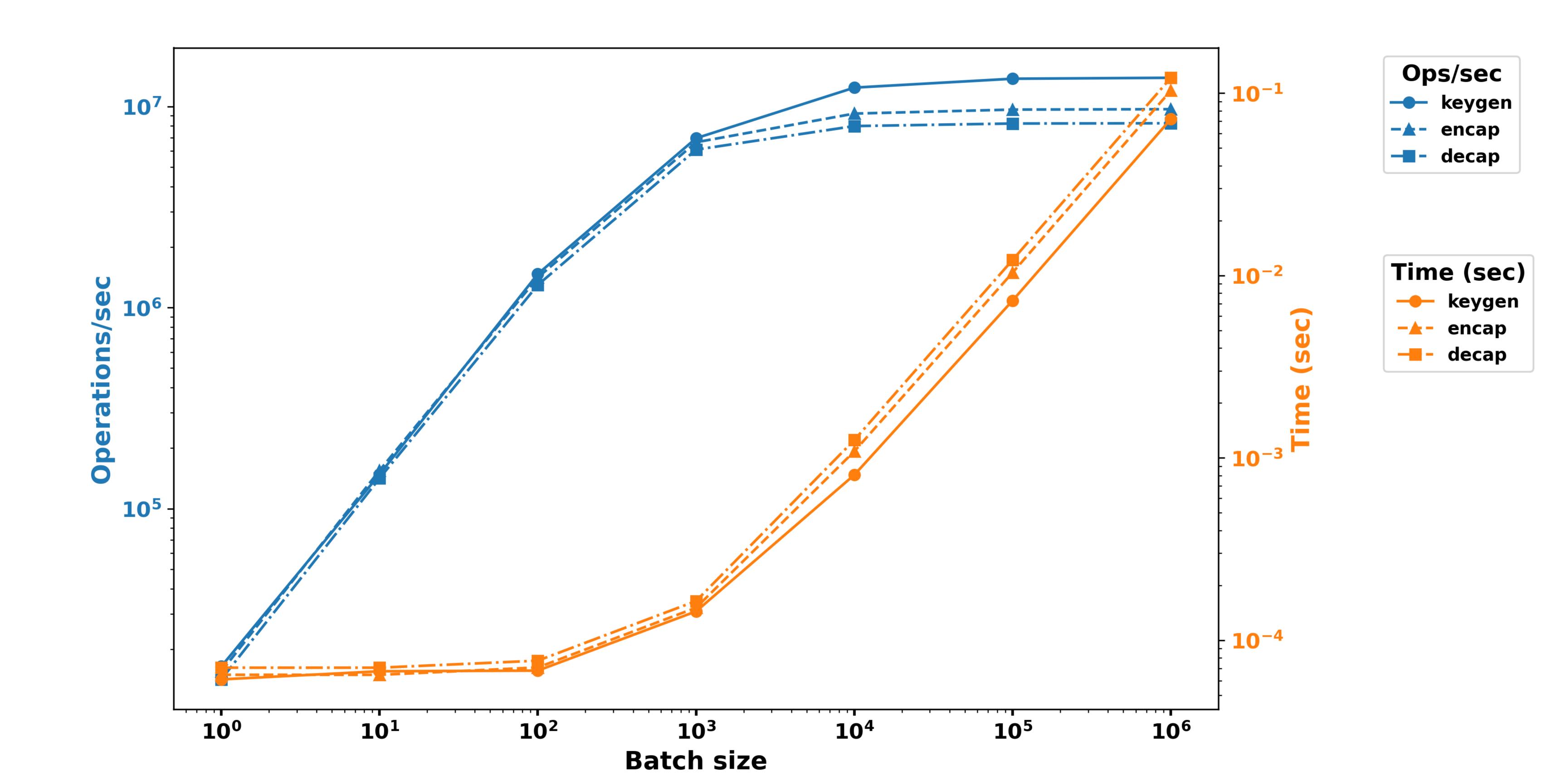
GPU Parallelism: Natural Noise Enhances Security Against Side-Channels





More resistant to side-





ML-KEM Benchmarks

ML-KEM-768



Keygen

| Security Level | Amortized GPU Time (µsec) | Operations/sec (in Millions) |
|----------------|------------------------------|---------------------------------|
| ML-KEM-512 | 0.049 | 20.36 |
| ML-KEM-768 | 0.072 | 13.88 |
| ML-KEM-1024 | 0.088 | 11.35 |



ML-KEM (Batched in 1,000,000)

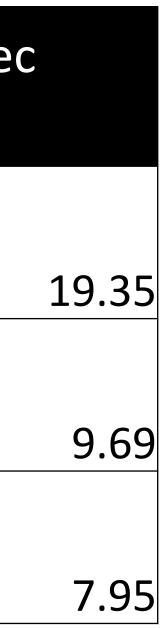


Decapsulation

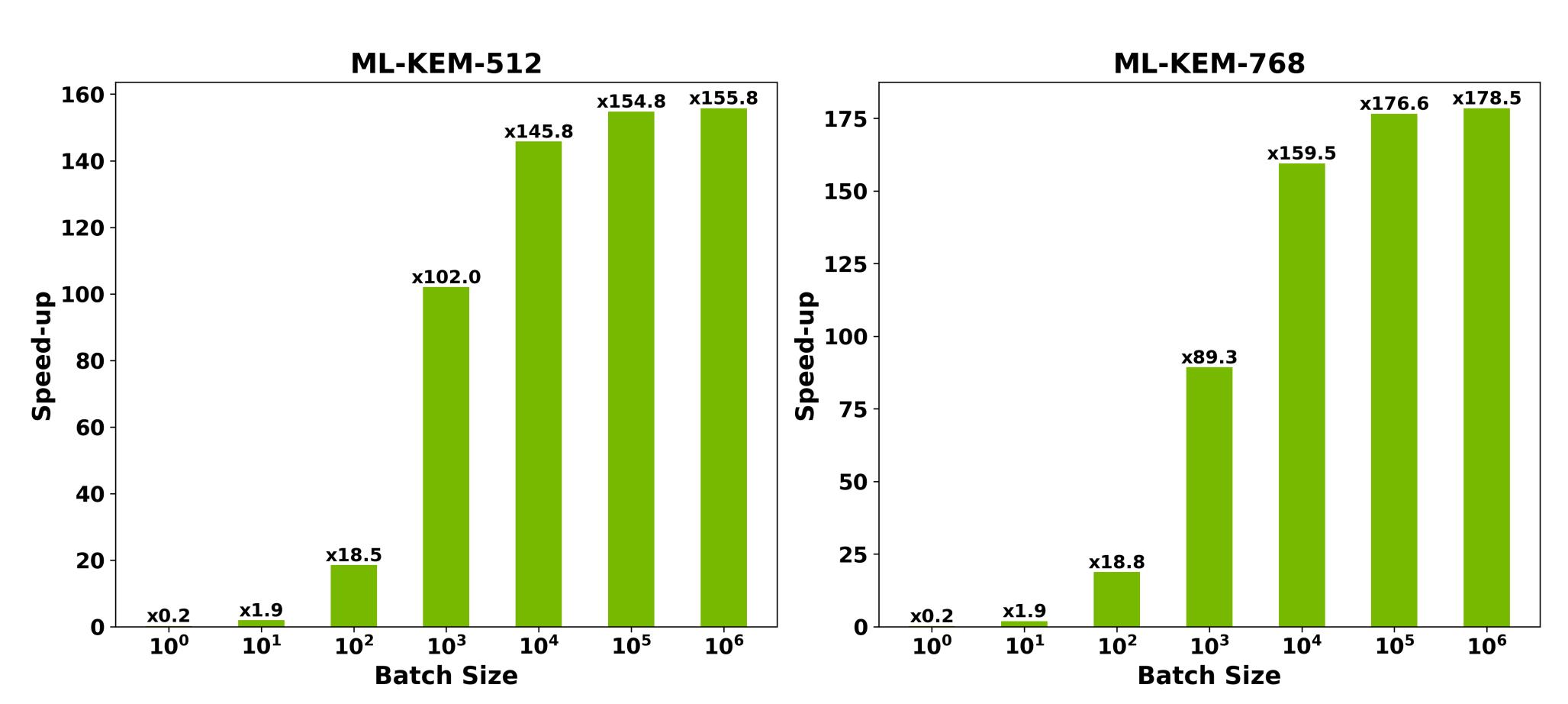
| Security Level | Amortized GPU Time (µsec) | Operations/sec (in Millions) |
|----------------|------------------------------|---------------------------------|
| EM-512 | 0.055 | 18.21 |
| EM-768 | 0.121 | 8.25 |
| EM-1024 | 0.133 | 7.47 |

Encapsulation

| vel | Amortized GPU Time (μ sec) | Operations/sec (in Millions) |
|-----|---------------------------------|---------------------------------|
| | 0.051 | |
| | 0.103 | |
| | 0.125 | |

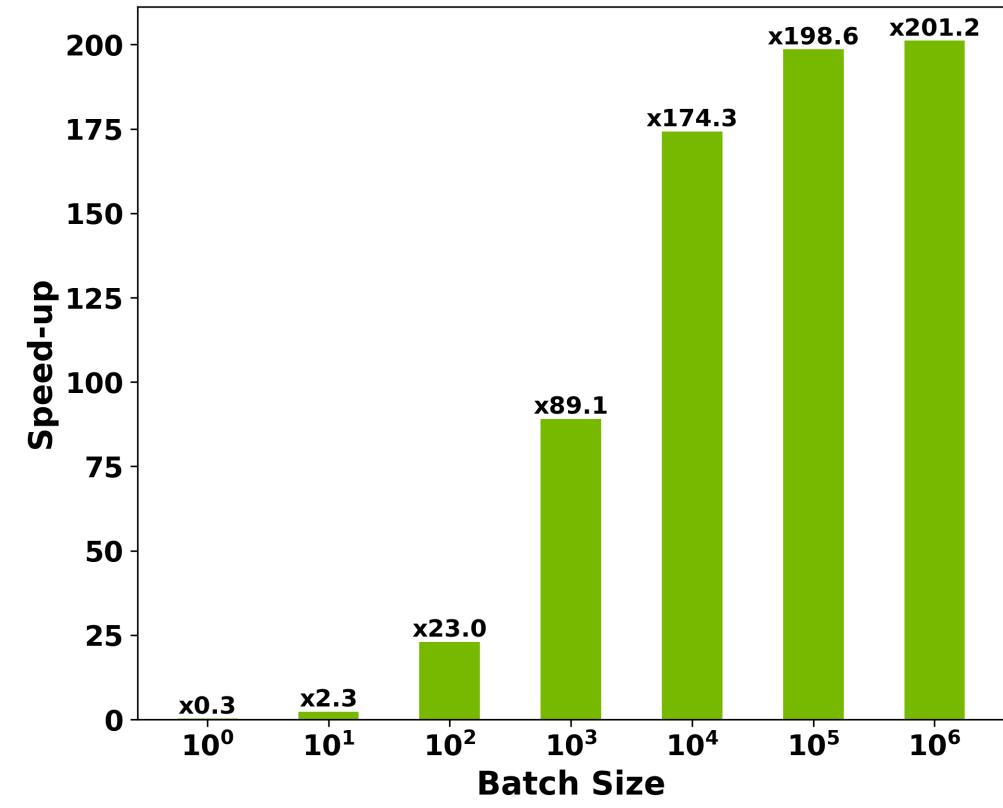




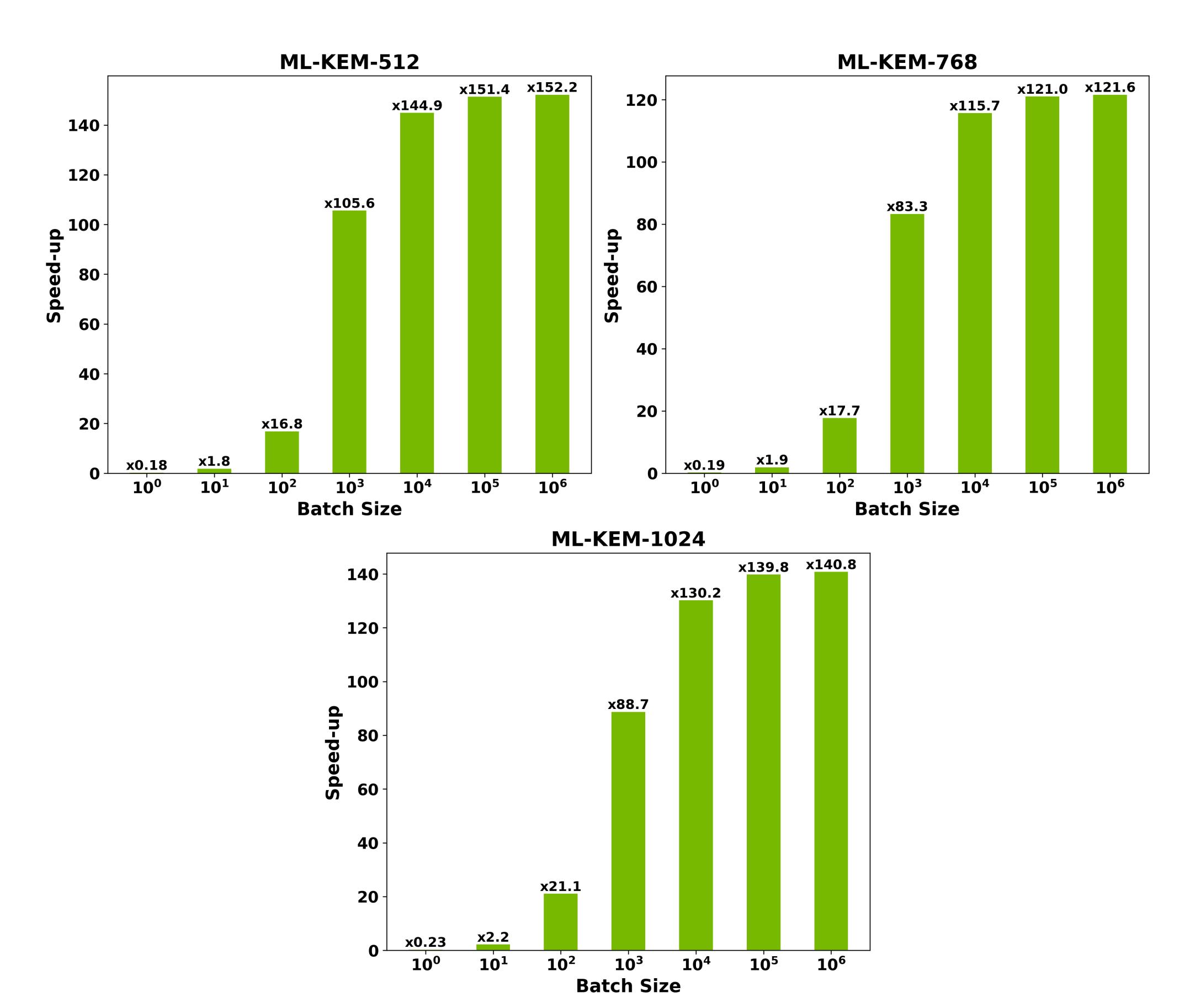


ML-KEM Keygen Benchmarks AMD EPYC 7313P 16-Core Processor vs NVIDIA H100 SXM5

ML-KEM-1024

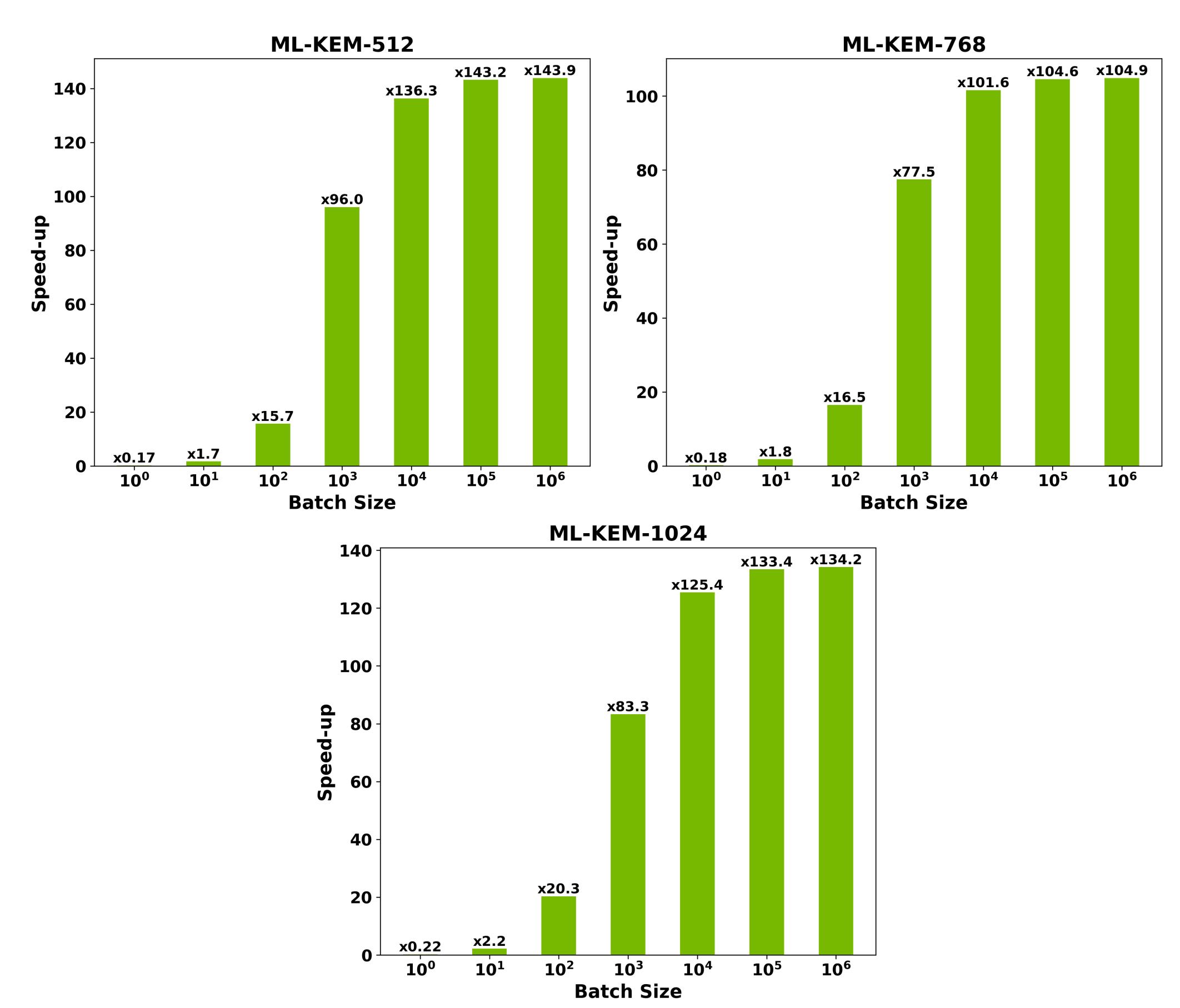






ML-KEM Encapsulation Benchmarks AMD EPYC 7313P 16-Core Processor vs NVIDIA H100 SXM5

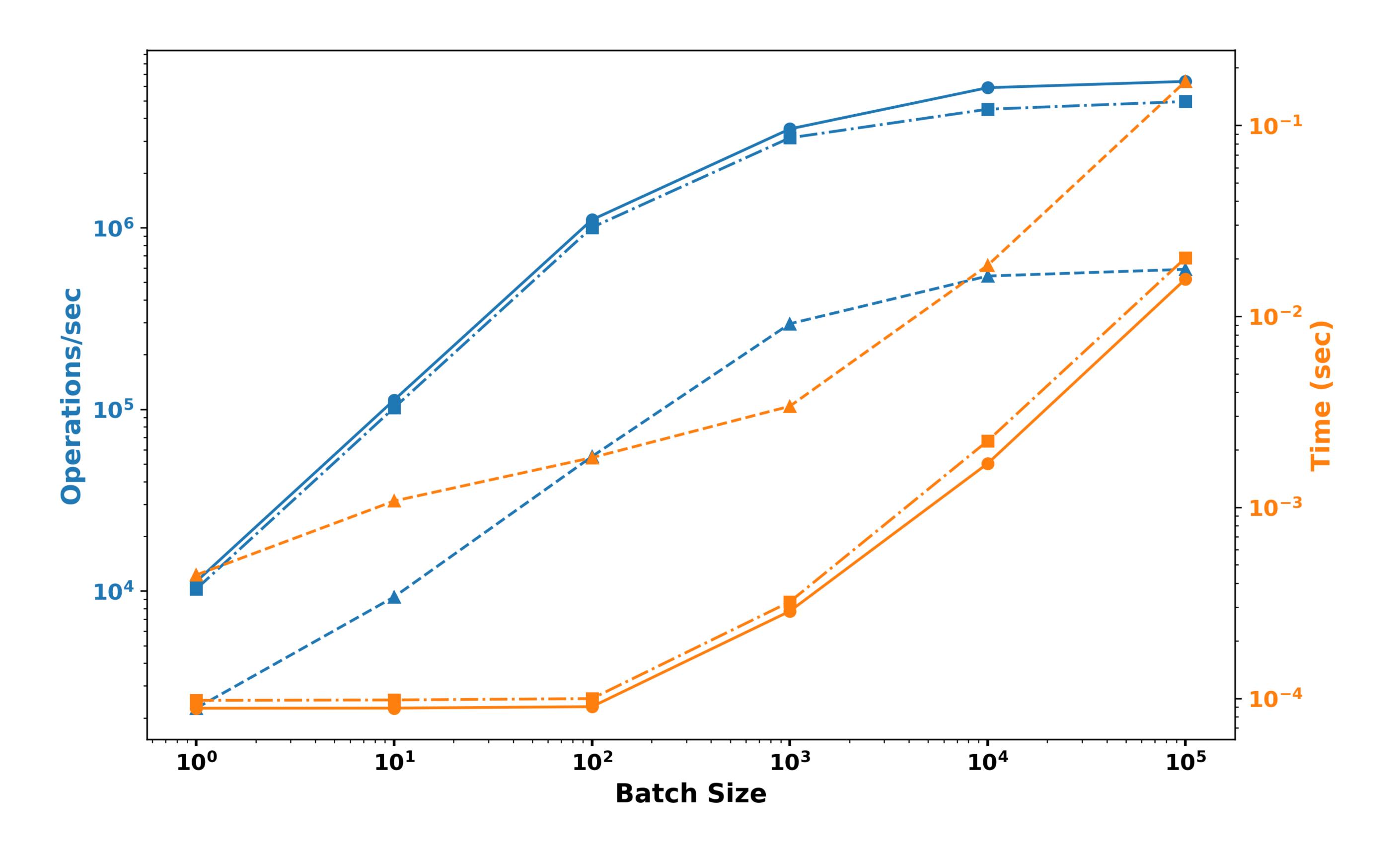




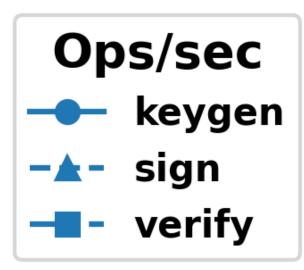
ML-KEM Decapsulation Benchmarks

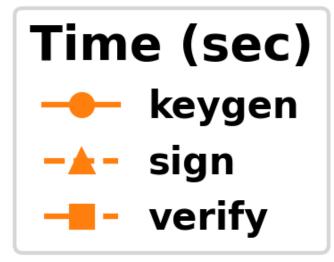
AMD EPYC 7313P 16-Core Processor vs NVIDIA H100 SXM5





ML-DSA-65

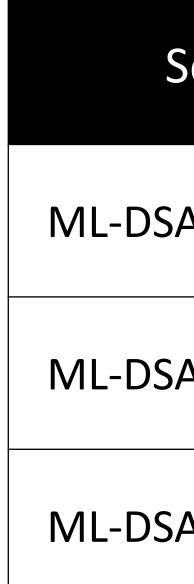






Keygen

| Security Level | Amortized GPU Time (µsec) | Operations/sec (in Millions) | Security Leve |
|----------------|------------------------------|---------------------------------|---------------|
| ML-DSA-44 | 0.12 | 8.21 | ML-DSA-44 |
| ML-DSA-65 | 0.16 | 6.38 | ML-DSA-65 |
| ML-DSA-87 | 0.23 | 4.32 | ML-DSA-87 |



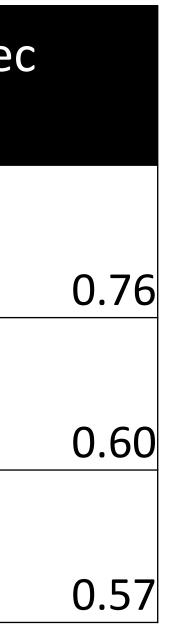
ML-DSA (Batched in 100,000)

Verify

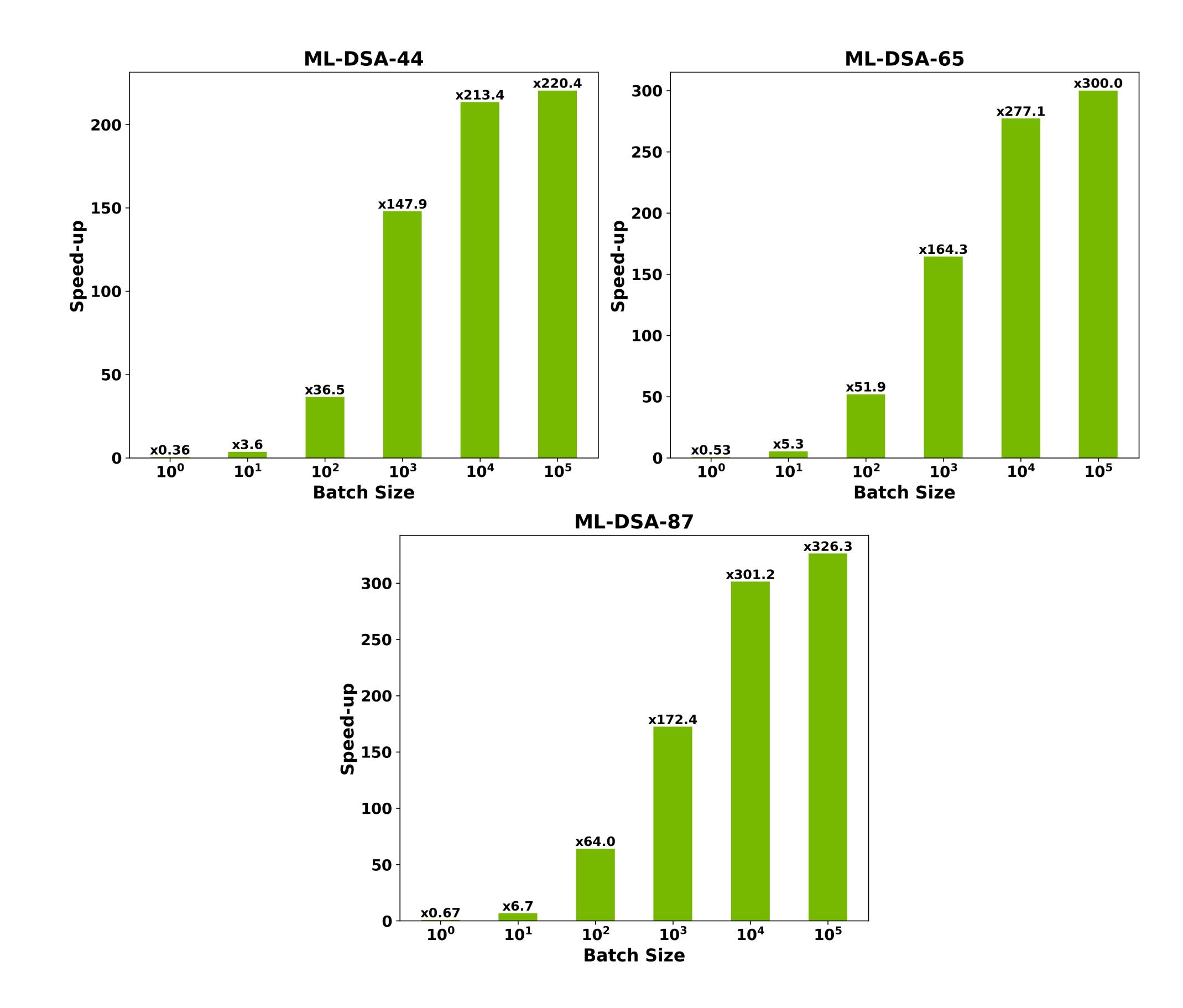
| Security Level | Amortized GPU Time (μ sec) | Operations/sec (in Millions) |
|----------------|---------------------------------|---------------------------------|
| SA-44 | 0.136 | 7.35 |
| SA-65 | 0.202 | 4.95 |
| SA-87 | 0.285 | 3.50 |

Sign

| 'el | Amortized GPU Time (µsec) | Operations/sec (in Millions) |
|-----|------------------------------|---------------------------------|
| | 1.30 | |
| | 1.70 | |
| | 1.76 | |



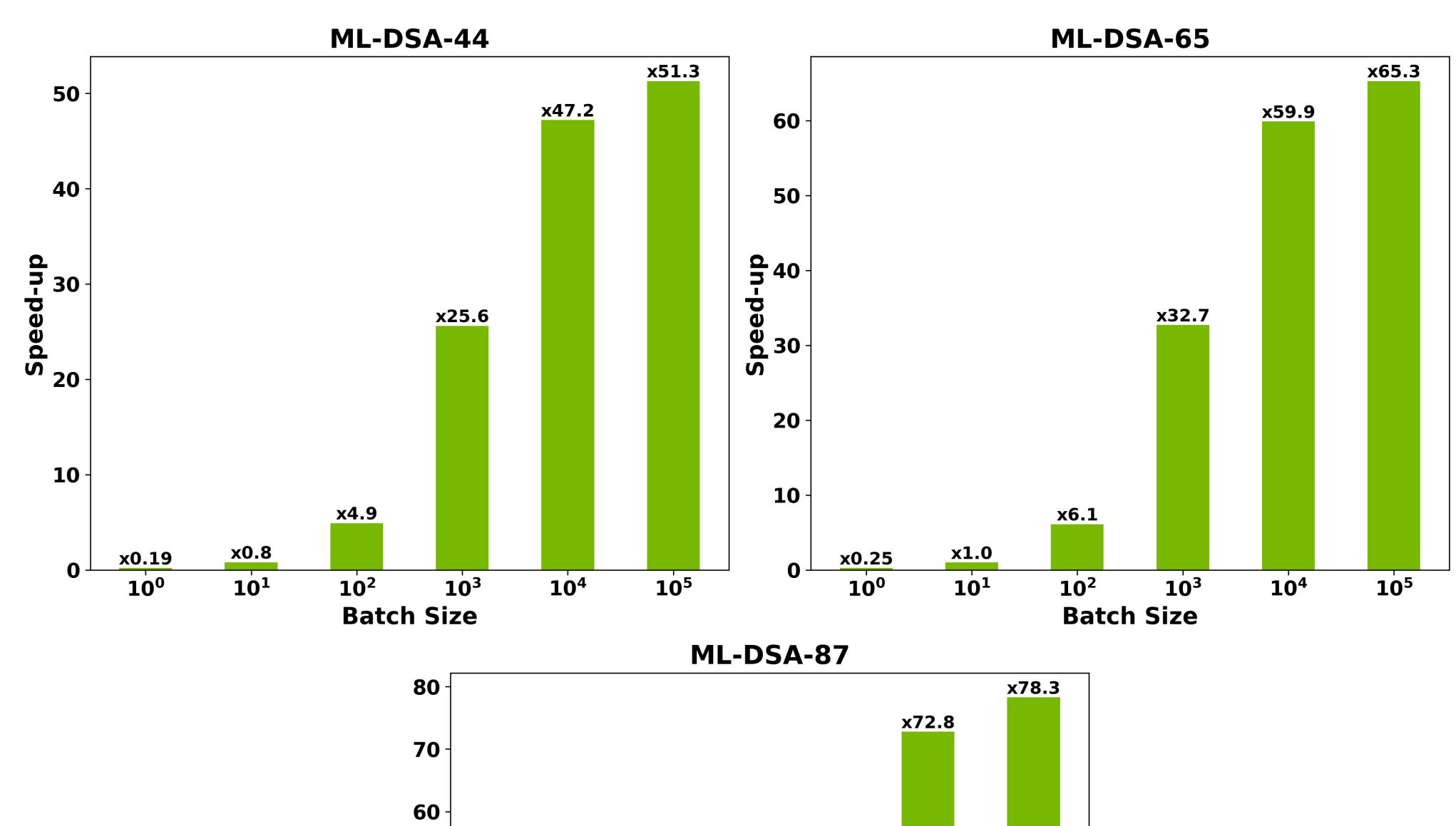




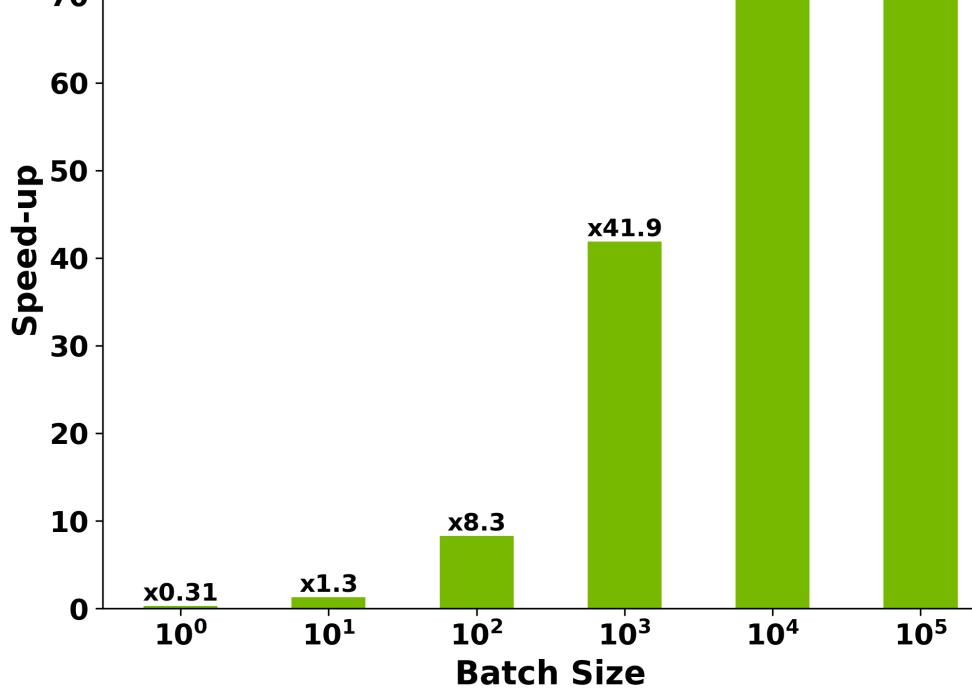
ML-DSA Keygen Benchmark AMD EPYC 7313P 16-Core Processor vs NVIDIA H100 SXM5



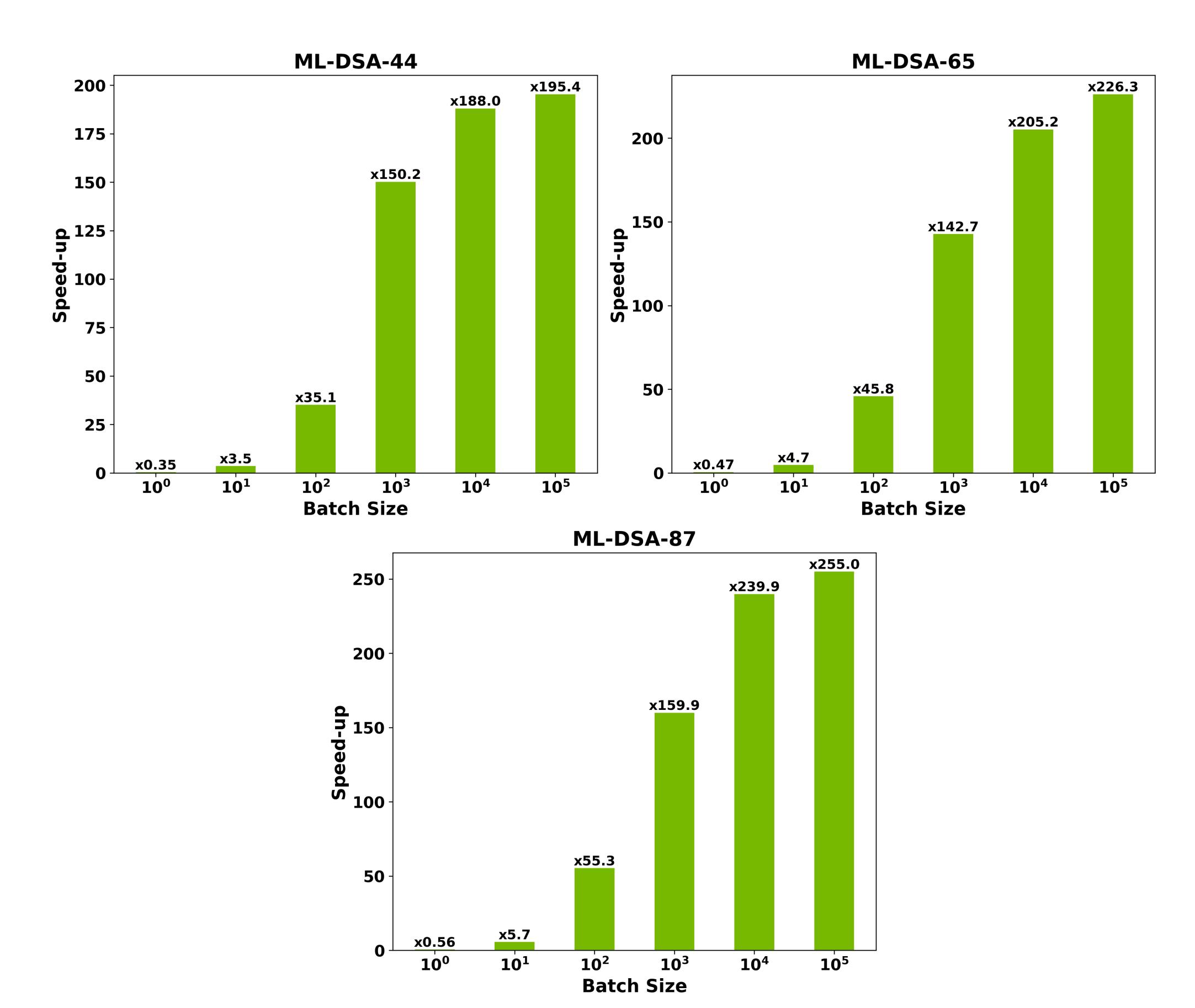




ML-DSA Sign Benchmark AMD EPYC 7313P 16-Core Processor vs NVIDIA H100 SXM5







ML-DSA Sign Verify Benchmark AMD EPYC 7313P 16-Core Processor vs NVIDIA H100 SXM5





Thank You!





Questions?

